Code No: 153AN **R18**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B. Tech II Year I Semester Examinations, September/October - 2023
DIGITAL SYSTEM DESIGN
(Electronics and Communication Engineering)

Time: 3 Hours **Max. Marks: 75**

Note: i) Question paper consists of Part A, Part B.
ii) Part A is compulsory, which carries 25 marks. In Part A, answer all questions.
iii) In Part B, Answer any one question from each unit. Each question carries 10 marks and may have a, b as sub questions.

PART-A

(25 Marks)

1.a) Given that $(292)_{10} = (1204)_b$, determine the value of b. [2]
b) Place the equation $(A + \bar{B} + C)(\bar{A} + D)$ into proper minterm or maxterm canonical form. [3]
c) Describe the importance of don't care conditions. [2]
d) Implement half Adder using NAND Gates. [3]
e) State the need for preset and clear inputs of a flip-flop. [2]
f) Define asynchronous circuits. List any two drawbacks of asynchronous circuits. [3]
g) Differentiate fundamental mode and pulse mode asynchronous sequential circuits. [2]
h) What is ASM? Give the basic notations. [3]
i) Describe the specifications (i) Fan in and Fan out and (ii)Noise margin. [2]
j) Compare TTL, ECL and CMOS. [3]

PART-B

(50 Marks)

2.a) How to detect and correct the error in the hamming code? Encode a binary word 11001 into the even parity hamming code.
b) Define and write about pros and cons of canonical form and differentiate with standard form. Express the Boolean function F = A + B'C as standard sum of minterms. [5+5]

OR

3.a) Find the standard sum of products (SOP) for the logic expression:
$F(A, B, C, D) = A\bar{B} + \bar{A}B\bar{C} + B\bar{C}D$
b) Convert the following logic system into NOR gates only. As shown in figure 1. [5+5]

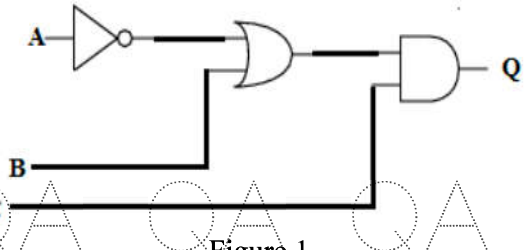

Figure 1

4.a) Using a 4 variable K map, simplify, F (A, B, C, D) = ∑m (1,4,9,10,11,12,14) + d (0,8,13) Realize the function using NAND gates only.
b) Implement the following Boolean functions with a multiplexer:
F(w,x,y,z) = ∑(2,3,5,6,11,14,15). [5+5]

OR

5.a) Simplify the following switching functions using Quine McCluskey's tabulation method and realize expression using gates F (A, B, C, D) = Σ (0,5,7,8,9,10, 11, 14,15).

b) Design a logic circuit that accepts a 4-bit gray code and converts it into 4-bit binary code. [5+5]

6.a) Discuss about static, dynamic and essential hazards in asynchronous sequential circuits.

b) Develop the logic circuit diagram and table for 4 -bit ring counter and explain the working. [5+5]

OR

7.a) What is the drawback of JK flip-flop? How is it eliminated in Master Slave flip-flop? Explain with diagram.

b) Explain the difference between Ring and Johnson counters with neat sketch. [5+5]

8.a) Explain Mealy and Moore model of a clocked synchronous sequential network.

b) Design a clocked synchronous sequential logic circuit for the following state diagram. Use state reduction if possible, using D flip flops. As shown in figure 2. [4+6]

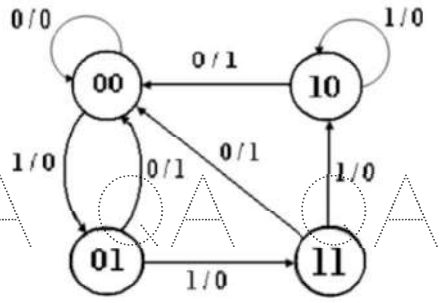

Figure 2

OR

9.a) Define state, present state, state diagram and state table.

b) Draw and explain the working of mod-18 counter using D-type flip-flop. [4+6]

10.a) Explain the working of open collector TTL NAND gate with circuit diagram.

b) Derive and discuss about CMOS dynamic electrical behaviour with characteristics. [5+5]

OR

11.a) What is meant by Tristate logic? Draw the circuit of Tristate TTL logic and explain the functions.

b) Explain about TTL to CMOS interfacing. [5+5]

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